

# Etching Techniques for Thinning Silicon Wafer for Ultra Thin High Efficiency Interdigitated Back Contact Solar Cells

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**Abstract** High efficiency Interdigitated back contact (IBC) solar cells help reduce the area of solar panels needed to supply sufficient amount of energy for household consumption. We believe that a properly passivated IBC cell with the aid of light trapping schemes can maintain an efficiency of 20% even with thickness under 20  $\mu\text{m}$ . In this work, photolithography and etching techniques are used for deep etching of crystalline Silicon (c-Si) wafer to a thickness less than 20  $\mu\text{m}$ . Tetramethylammoniumhydroxide (TMAH) wet anisotropic etching and plasma based Reactive ion etching (RIE) are used with SPR 220-7.0 and SU-8 photoresists.  $\text{SiO}_2$  is used as making layer for TMAH etching. TMAH etch of a 4-inch c-Si wafer is done at a temperature of 80°C for 8 hours. RIE of a quarter of a 4-inch c-Si wafer is done for 3 hours using  $\text{SF}_6$  as reactive gas. A baseline photolithography process flow for SU-8 photoresist deposition was developed. The etch rates of TMAH etch techniques fall within the range of 0.3 – 0.45  $\mu\text{m}/\text{min}$  and etch rates for RIE fall within the range of 1.2 – 1.8  $\mu\text{m}/\text{min}$ . The RIE shows capability of achieving smaller thickness sizes with greater advantages than the TMAH etching technique.

**Keywords:** IBC solar cells, masked etching, photolithography, reactive-ion etch, and tMAH etching

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## 1. Introduction

Higher efficiency solar cells have been reported to give efficiencies greater than 20% on a scale higher than the commercially available solar cells using crystalline silicon material. One of these types of PV cells is the Interdigitated Back Contact Solar cell [1,2].

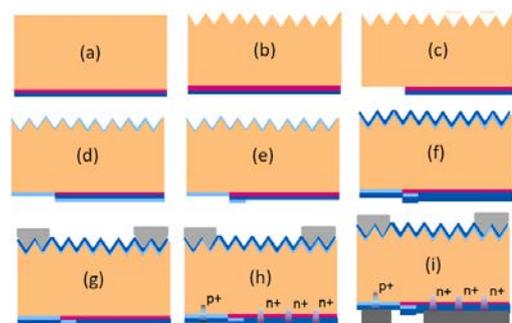
IBC solar cells are cells with both p+ contacts and n+ emitters on the rear side of the cell which prevents shading losses. The metallization on the rear side of these cells follow an interdigitated patterning. The advantages of this type of cell are: (a) there are no metal shadow losses in the front side (b) resistive losses due to the fingers and busbar can be very low, and (c) there is easier cell interconnection [3,4].

IBC solar cells allow further reduction of cell thickness with the aid of light trapping schemes in crystalline silicon cells such as anti-reflection coatings and random texturing, which helps in increasing absorption of carriers, the total internal reflections and also the percentage of light absorbed, thereby maintaining high efficiency. This means that a well passivated IBC solar cell through these light trapping schemes can maintain efficiency up to 20% even with thickness under 20  $\mu\text{m}$  [5].

IBCs were introduced to increase conversion efficiency of crystalline silicon solar cells greater than 20%. With this high efficiency, the size of panels 6.5  $\text{m}^2$  of traditional cells can be reduced to 4.8  $\text{m}^2$  or less to meet the total

family average annual energy demand. The major goal is to develop procedures that facilitate large scale production [4].

The IBC cell at UPC is processed by surface passivation of Aluminium oxide/amorphous Silicon Carbide ( $\text{Al}_2\text{O}_3/\text{a-SiC}_x$ ) for p+ contact, phosphorus-doped silicon carbide stack/Hydrogenated amorphous Silicon Carbide ( $\text{SiC}_x/\text{a-Si:H}$ ) for the n+ contact and a-SiC<sub>x</sub> as the back reflector. The contacts are created by laser processing and Aluminium metallization of the rear side to complete the fabrication process [3,6,7,8]. The baseline fabrication process of an IBC-BJ solar cell at UPC is shown in Figure 1.



**Figure 1.** The baseline fabrication process of an IBC-BJ Solar cell (a) a:Si(i) 5 nm + 20 nm, a:Si(n) + 25 nm  $\text{SiC}_x$  deposition (back) (b) Etching of front surface using desired etching (c) Stack etching ( $\text{CF}_4$  4 min and wet etching 3 min) (d)  $\text{Al}_2\text{O}_3$  deposition (90 nm) (e)  $\text{Al}_2\text{O}_3$  selective wet etching (back) (f)  $\text{SiC}_x(\text{i})$  deposition (back 50 nm front) (g) Al deposition lift-off (e-beam) front 0.3  $\mu\text{m}$  and annealing 400°C 10 min (h) Laser stage (19.8A 6 pulses 250  $\mu\text{m}$  pitch) (i) Ti/Al metallization (35 nm/4000 nm) e-beam, annealing T = 350°C 10 min [6,7]

The idea of the work is to improve the baseline process by using the most efficient etching technique (step b) to optimize the fabrication process and also miniaturize the already available 250  $\mu\text{m}$  thick IBC solar but still maintaining the efficiency greater than 20% in the future [6,7].

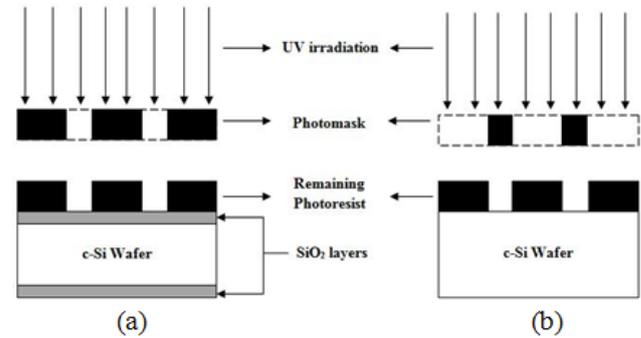
In order to achieve this and experimentally demonstrate this idea, we try to develop reliable procedures to deeply etch silicon wafers to a thickness less than 20  $\mu\text{m}$ . Technological trends have been widely used to etch silicon wafers. Anisotropic wet etching has been an extensively used technique for microstructure fabrication on silicon wafers because of its IC compatibility and also it is cheaper to implement. Tetramethylammoniumhydroxide (TMAH) is used as the anisotropic etchant in this work [2,9,10,11]. Recent developments introduce dry etching, more especially the plasma-based technique known as Reactive Ion Etching. RIE involves a combination of physical mechanism (ion bombardment) and chemical mechanism (chemical reaction of etchant gases) to produce a more anisotropic etch profile [12].

This paper presents the use of the RIE technique to thin Silicon wafers to a final thickness less than 20 microns. This was achieved by using SU-8 photoresist, a high contrast negative epoxy based photoresist as masking layer. A study was carried out on the behavior of this type of Photoresist at thin film deposition thickness of 6 microns, 40 microns and 120 microns. A baseline photolithography process was developed using SU-8 photoresist. The outcome of using SU-8 and RIE method was compared to the popular anisotropic wet chemical etching in terms of the etch profile and most especially the etch rates. The understanding of this concept is useful for future applications in the fabrication of ultra thin IBC solar cells by miniaturizing bulky silicon wafers used in the manufacturing process.

## 2. Experiment

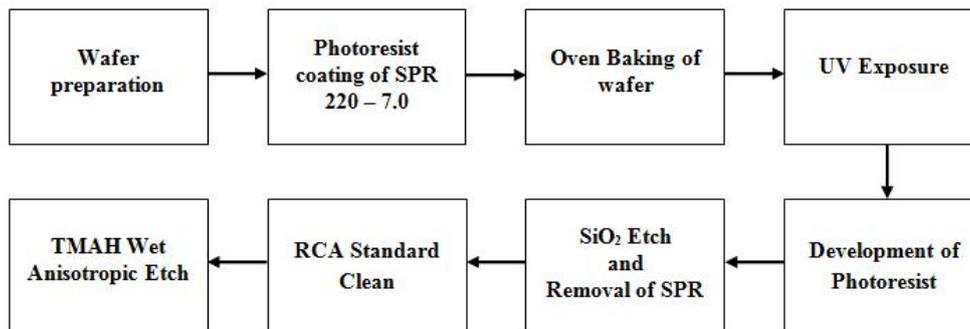
100nm thin layer of thermally deposited  $\text{SiO}_2$  was coated on both sides of a (100) oriented crystalline Silicon wafer (4 inches) and pre-treated with acetone and isopropyl solutions, and then rinsed and dried with water and  $\text{N}_2$  respectively. The wafer of this type has a thickness ranging between 260  $\mu\text{m}$  and 290  $\mu\text{m}$ . Thin film deposition

on the wafer was done using a Megaposit 220-7.0 SPR positive photoresist. This positive photoresist is removed from areas where there is no masking because UV irradiation softens the unmasked areas of SPR. The opposite is the case for the negative photoresist [13]. These behaviors are portrayed in Figure 2.



**Figure 2.** Response of (a) SPR positive photoresist and (b) SU-8 negative photoresist to UV irradiation

The wafer with SPR is baked in an oven for 15 mins at a temperature of 105°C and cooled for a few minutes before exposing to UV irradiation to create windows on the surface of the substrate. A hold time of 45 minutes before developing using Megaposit Developer MF24A to remove the SPR from the windows created for etching. A thin layer of  $\text{SiO}_2$  on the silicon surface is etched in Ammonium Fluoride etching mixture solution with SPR as masking for the  $\text{SiO}_2$ . SPR is removed from the surface and RCA standard clean steps are performed on this sample to remove organic residues from the surface. This is done in a solution of 5 parts of deionized water ( $\text{H}_2\text{O}$ ), 1 part of aqueous  $\text{NH}_4\text{OH}$  (29% by weight of  $\text{NH}_3$ ) and 1 part of aqueous  $\text{H}_2\text{O}_2$  (Hydrogen peroxide, 30%) at a temperature of 70°C for a period of 10 mins. The wafer is washed and dried with  $\text{H}_2\text{O}$  and  $\text{N}_2$ . The substrate is inserted in a 23% concentration of TMAH at an etching temperature of 80°C for 8 hours in order to etch the windows on one side (front side) of the wafer. The 8 hours time duration is divided into smaller times to check the etch rates. The process flow of the SPR deposition and TMAH etching is shown in Figure 3. This process was repeated on a wafer with SPR 7.0 on both sides to mask the  $\text{SiO}_2$  on the rear side during  $\text{SiO}_2$  etch.



**Figure 3.** SPR Photolithography and TMAH Process Flow (from wafer preparation, SPR coating, Oven baking of wafer, UV exposure, SPR development,  $\text{SiO}_2$  etch and SPR removal, RCA standard clean to the final TMAH anisotropic etch process)

Another wafer is divided into four parts and each quarter is used to perform an SU-8 deposition to show a repeated process. The SU-8 photoresist is chemically and

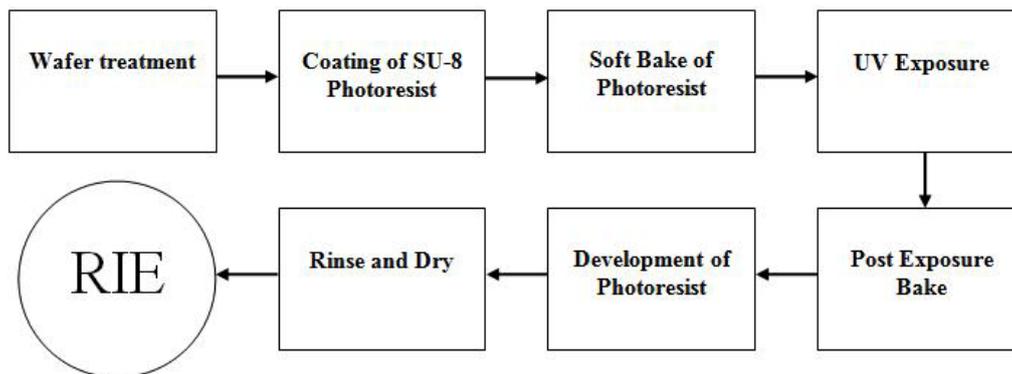
thermally stable with excellent imaging characteristics. 40 microns film thickness is deposited on the substrate and baked for 7 minutes on a hot plate. UV irradiation is

exposed to the sample to form an image. The photoresist remains on the area where there is no masking as shown in Figure 2(b). A post exposure bake is done before developing with an SU-8 developer for 7 minutes, and then cleaned with isopropyl solution for 10 seconds. The substrate is rinsed and dried with water and N<sub>2</sub>. This

process is done for a thickness of 120 microns on a full wafer with different parameters. The parameters used to perform SU-8 deposition and photolithography for 6, 40 and 120 microns are summarized in Table 1. The process flow for SU-8 deposition is shown in Figure 4.

**Table 1. Photolithography parameters for 40 and 120 microns SU-8 deposition**

Parameters		6 $\mu\text{m}$	40 $\mu\text{m}$	120 $\mu\text{m}$
<b>SU-8 Photoresist Series</b>		SU-8 2005	SU-8 2050	SU-8 2050
<b>Spin Coating</b>	<b>Spin Speed</b>	1 <sup>st</sup> Cycle	500 rpm	500 rpm
		2 <sup>nd</sup> Cycle	2000 rpm	4000 rpm
	<b>Acceleration</b>	1 <sup>st</sup> Cycle	100 rpm/sec	100 rpm/sec
		2 <sup>nd</sup> Cycle	300 rpm/sec	300 rpm/sec
<b>Soft Bake</b>	<b>Bake Temperature</b>	95°C	95°C	95°C
	<b>Bake Time (Duration)</b>	2 mins	7mins	22mins
<b>Alignment and UV Exposure</b>	<b>Exposure Power</b>	270 mJ/cm <sup>2</sup>	270 mJ/cm <sup>2</sup>	270 mJ/cm <sup>2</sup>
	<b>Number of Cycles</b>	1	2	2
	<b>Exposure Time per cycle (Total)</b>		20 s	20 s
				(40 s)
<b>Post Exposure Bake</b>	<b>Bake Temperature</b>	95°C	95°C	95°C
	<b>Bake Time (Duration)</b>	3 mins	7 mins	11 mins
<b>Development</b>	<b>Development Time</b>	3 mins	7 mins	10 mins



**Figure 4.** Photolithography and RIE process Flow for SU-8 deposition (from wafer treatment and preparation, PR coating, Thermal baking, UV Exposure, PEB, PR development to the final RIE process)

**Table 2. RIE parameters for c-Si etching**

Parameter	Conditioning and Process Chamber
Gases	SF <sub>6</sub> (45 sccm)
Pressure	15 mTorr
Power	15 W
ICP	800 W
Temperature	20°C

RIE was used to etch (100) oriented crystalline silicon wafer in order to determine the etch rates and characterize this etching process. RIE system consists of a cylindrical vacuum chamber with a combination of a parallel plate reactor powered by a 13.56 MHz radio frequency (RF) generator. The wafer is placed on a cooled surface (20°C) power electrode of the parallel plate reactor and negative DC bias generated in the electrode where the substrate was placed, exposing the wafer to the bombardment of positive ions. Sulfur Hexafluoride (SF<sub>6</sub>) is the reactive gas used and are fed into the chamber. SF<sub>6</sub>, which is used for silicon etching experiences dissociation as a result of gas

discharge, thereby generating fluorine ions used for etching. The wafer is held in the chamber by a process known as Helium backing. In this work, the RIE was divided into two steps: (1) Conditioning chamber step (SF<sub>6</sub> test on dummy substrate) (2) Process Chamber (SF<sub>6</sub> on substrate). The etch conditions depend on the process parameters including the pressure, gas flows, RF power and summarized in Table 2.

Etch was done for a total time of 3 hours in steps of 1 hour to calculate the etch rates per hour. The remaining photoresist was removed with 1-methyl-2-pyrrolidone at a temperature of 120°C on the hot plate and SU-8 deposition is done on the wafer after each hour of RIE because SU-8 becomes hard and parts of it wear off from the surface of the wafer after RIE.

The etch depth for each hour is measured by profilometry.

Compatibility tests were carried out on two sets of wafers with (a) the SU-8 on the front surface and the SPR on the rear side. (b) SU-8 and SPR on the same side (Front surface). The first case was to check if both photoresists are compatible for realization of the IBC fabrication, with

the oven at a temperature of 105°C for SPR on the rear side and 95°C for the SU-8 on the front side. The first case shows compatibility for IBC process. The second case was done to make the SU-8 remain on the surface of the wafer after the RIE. This case is not compatible because of the different responses of these two types of photoresists to UV irradiation and different photomasks.

### 3. Results and Discussion

#### 3.1. SPR Photoresist and TMAH Etching

A perfect anisotropic profile after performing the lithography with the SPR 220-7.0 photoresist is shown in Figure 5.

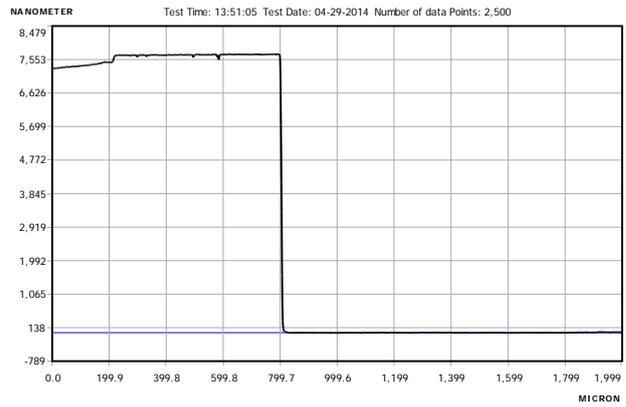
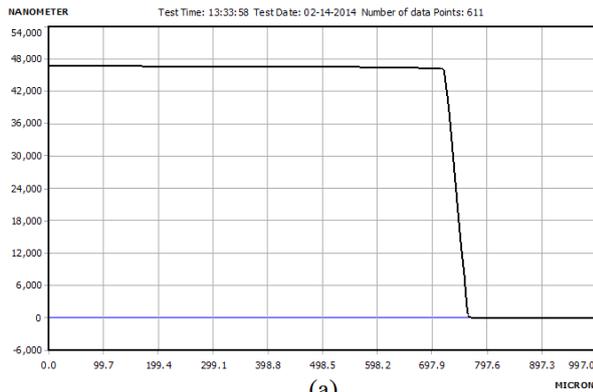
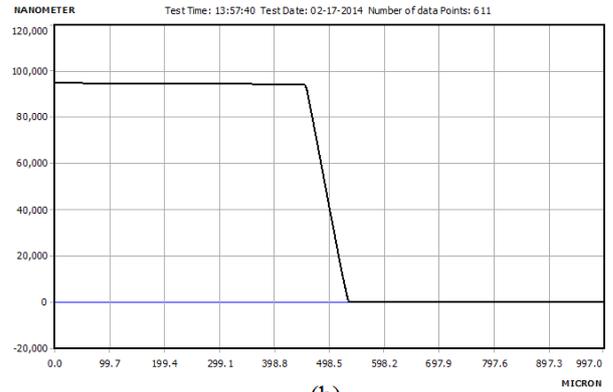


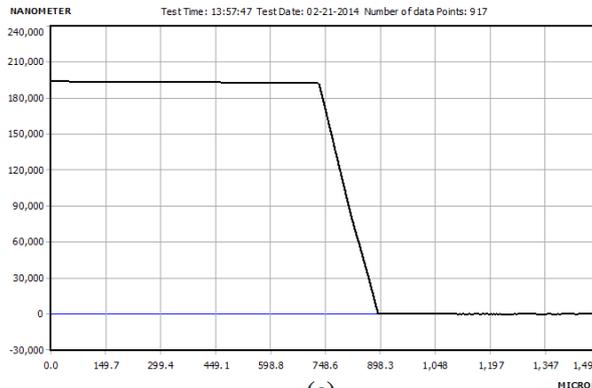
Figure 5. Surface profile of SPR 7.0 deposition ( $\approx 7 \mu\text{m}$  thickness)



(a)



(b)



(c)

Figure 6. Surface profile of etched wafer for (a) 2 hours (b) 4 hours (c) 8 hours TMAH etching

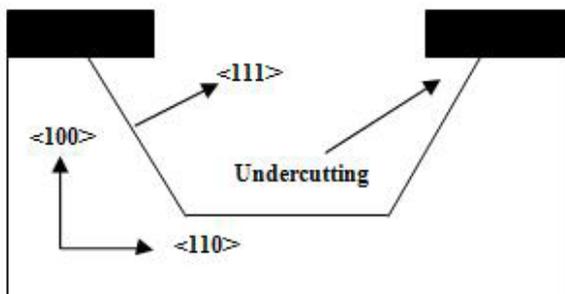


Figure 7. Tapered Anisotropic Etch profile of TMAH etch showing crystallographic orientations and undercutting effects

The case of the photoresist on one side of the sample, after 2 hours of TMAH etch, an etch depth of 46.6  $\mu\text{m}$  was obtained as shown in Figure 6 (a). After an extra 2 hour etch, the etch depth obtained was an extra 48.1  $\mu\text{m}$  making a total of 95  $\mu\text{m}$  etch after 4 hours as shown in Figure 6 (b). After another 4 hours of TMAH etching, a total of 8 hours

of etch. The final etch depth was 193.2 microns as shown in Figure 6 (c). The TMAH etch profile of silicon wafer has a tapered anisotropic etch profile forming a V-shape by the (111) oriented sidewalls as shown in Figure 7.

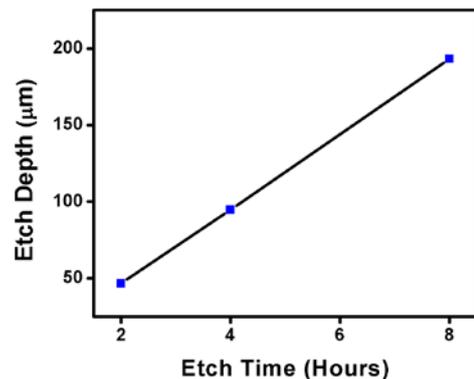


Figure 8. Etch rates (in  $\mu\text{m}/\text{min}$ ) of TMAH etching after 2 hours, 4 hours and 8 hours

The etch rates are calculated as Etch Depth/Etch time (in  $\mu\text{m}/\text{min}$ ) [14]. The etch rates for 2 hours, extra 2 hours

and finally 4 hours were 0.39, 0.40 and 0.41  $\mu\text{m}/\text{min}$  respectively. These values are plotted in Figure 8.

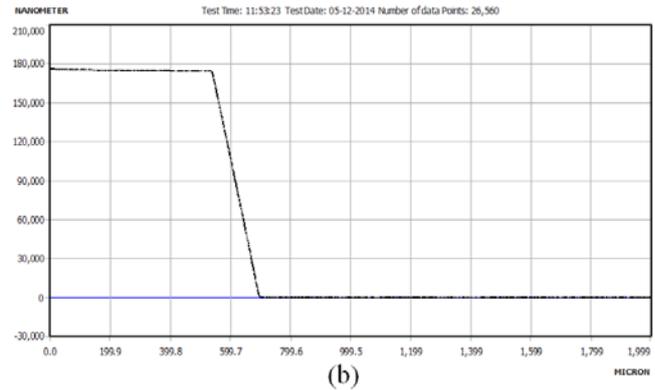
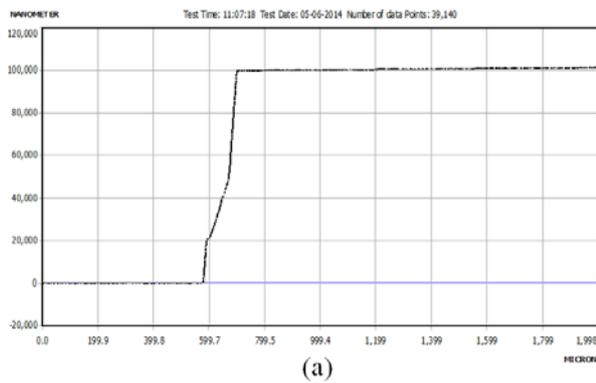


Figure 9. Surface profile of etched wafer for (a) 4 hrs 45 mins and (b) 3 hrs 15 mins of TMAH etching

The same experiment with SPR 7.0 on both sides of the wafer is done to evaluate repeatability and reliability of the process. After 4 hours 45 minutes of TMAH etch, the etch depth was 100.8  $\mu\text{m}$  as shown in Figure 9 (a). After an extra 3 hour 15 minutes of etch making a total of 8 hours, the etch depth was 175.3  $\mu\text{m}$  as seen in Figure 9 (b).

The same etch profile was observed as the first case. The etch rates for 4 hours 45 mins and 3 hours 15 minutes were 0.35  $\mu\text{m}/\text{min}$  and 0.37  $\mu\text{m}/\text{min}$ . These etch rates fall within the range of wet anisotropic etching, which is between 0.1 to 1  $\mu\text{m}/\text{min}$  [15]. The etch rates of (100) Silicon wafer can be improved by decreasing the concentration and increasing etching temperature [14,16].

Some problems were identified using TMAH etching techniques. After more than 4 hours of etch and exceeding a wafer thickness of 200 microns, pinholes were observed in the etched region using an optical microscope. Optical microscope images showing pinhole detection and calculation of its size are shown in Figure 10.

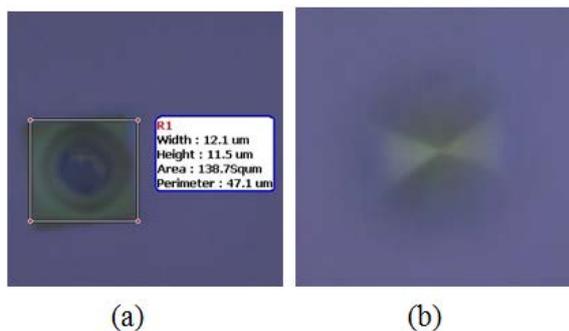


Figure 10. Optical Microscope images showing (a) Pinhole detection and measurement, Pinhole of dimension 12.1  $\mu\text{m} \times 11.5 \mu\text{m}$  with an area of 138.7 squm and 47.1  $\mu\text{m}$  perimeter was observed. (b) Vertex view of pinhole after closer zoom

The pinhole at a closer zoom appears like a vertex point as seen in Figure 10 (b) and contributes severely in reducing the cell yield strength and eventually leads to breakage [15,16,17]. This is a huge defect when fabricating high efficiency IBC solar cells. Larger pinholes and even breakage along the (110) crystallographic plane of the c-Si wafer were observed in the experiment of TMAH etching at lower thicknesses. It is necessary to check these defects before the wafer is introduced into further cell processing to avoid panel efficiency reduction.

Another problem noticed with the TMAH wet etching technique was the case of undercutting, whereby some

etches undercut the masking layer and form cavities beneath, forming sloping sidewalls [18] as shown in Figure 7. Undercutting of 1  $\mu\text{m}$  was observed for each 10  $\mu\text{m}$  of TMAH etch. Although this defect is more common with the isotropic etch (CP4 Etch, also called HNA – HF: Nitric: Acetic Etch).

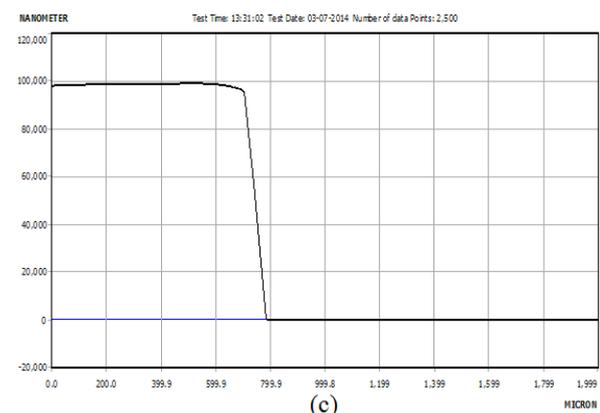
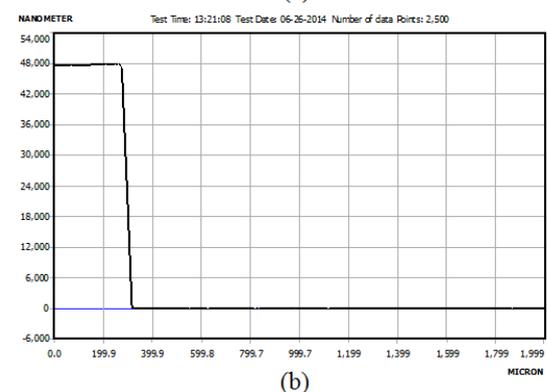
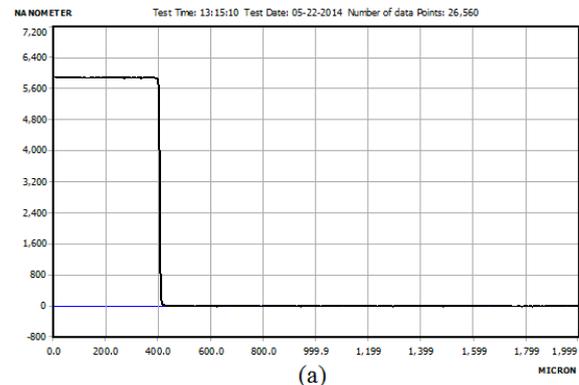


Figure 11. Surface profile of (a) 6  $\mu\text{m}$  (b) 40  $\mu\text{m}$  and (c) 120  $\mu\text{m}$  depositions

### 3.2. SU-8 Photoresist and RIE

The surface profile after performing the deposition and lithography with the SU-8 photoresist for 6 microns, 40 microns thickness and 120 microns thickness is shown in Figure 11 (a) – (c) respectively.

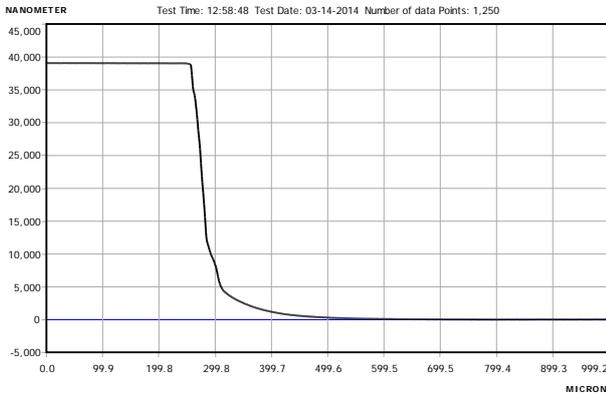
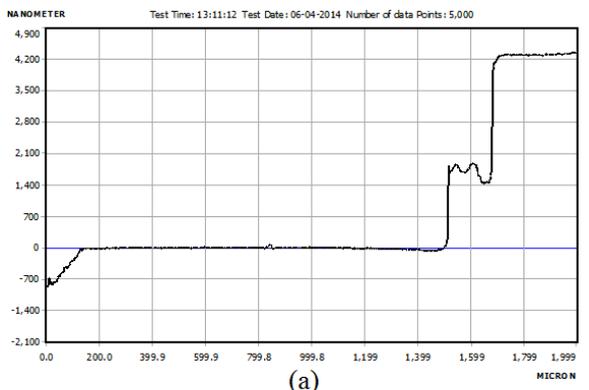
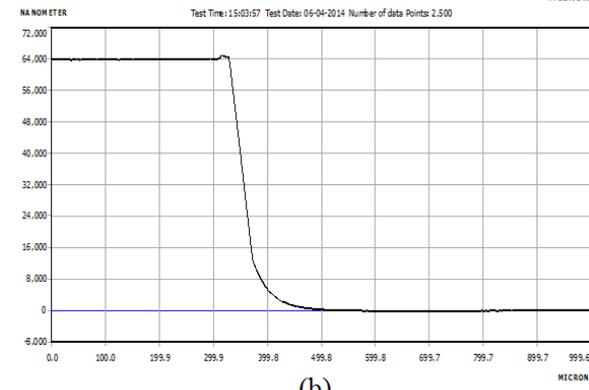
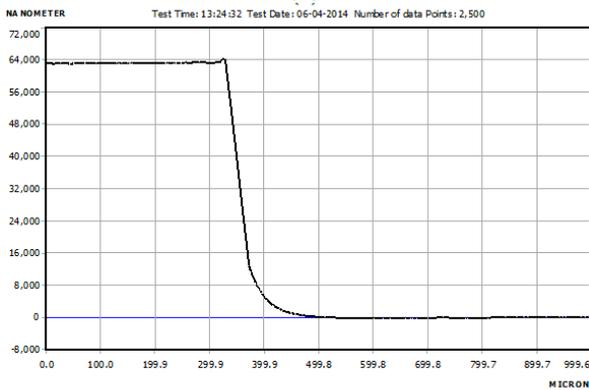


Figure 12. Surface profile of etched 120 μm deposited wafer after 1 hour of RIE



(a)



(b)

Figure 13. Surface profile of etched 6μm deposited wafer after 1 hour of RIE showing (a) Amount of SU-8 removed is 4.3μm. The final remaining SU-8 on the surface had a thickness of (6.0 – 4.3) μm = 1.7 μm. (b) Average Etch depth of 63.669 microns

For the case of 120 μm, after one hour of RIE and removal of SU-8 from the surface of the etch window of the wafer, the etch depth was 39 microns. This yields an etch rate of 0.65 μm/min (i.e. 39 microns/60 mins), which is less than 1 μm/min indicating a limited etch. This is shown in Figure 12.

The chamber clamp experiences problem holding the wafer. As a result of this, during the RIE, flux of Helium gas used in Helium backing was released inside the process chamber in excess, thereby mixing with the etchant gases leading to a reduction in the etch rate [19]. A smaller SU-8 deposition of 6 microns on a quarter of a wafer was used to perform the same experiment to avoid the previous problems. After one of hour of RIE of 6 microns deposited wafer, the SU-8 appeared to be completely removed. RIE is a very powerful etching technique, especially at high power. This means a large portion of a very small thickness deposition of photoresist can be completely removed from the surface during the etch process, thereby exposing protected areas to possible etching. It is observed that the remaining SU-8 protecting the surface of the wafer was 1.7 microns as shown in Figure 13(a). Removal of remaining SU-8 with 1-Methyl-2-Pyrrolidone yielded an average etch depth of 63.7 μm for one hour of RIE, giving an etch rate of 1.06 μm/min as shown in Figure 13 (b).

In order to achieve better etch results in terms of etch rates and wafer surface protection, 40 microns deposition on a quarter wafer was used to perform the same experiment. After one hour of RIE of 40 microns deposited wafer, the etch depth was 105.6 microns after taking an average of two sides as shown in Figure 14.

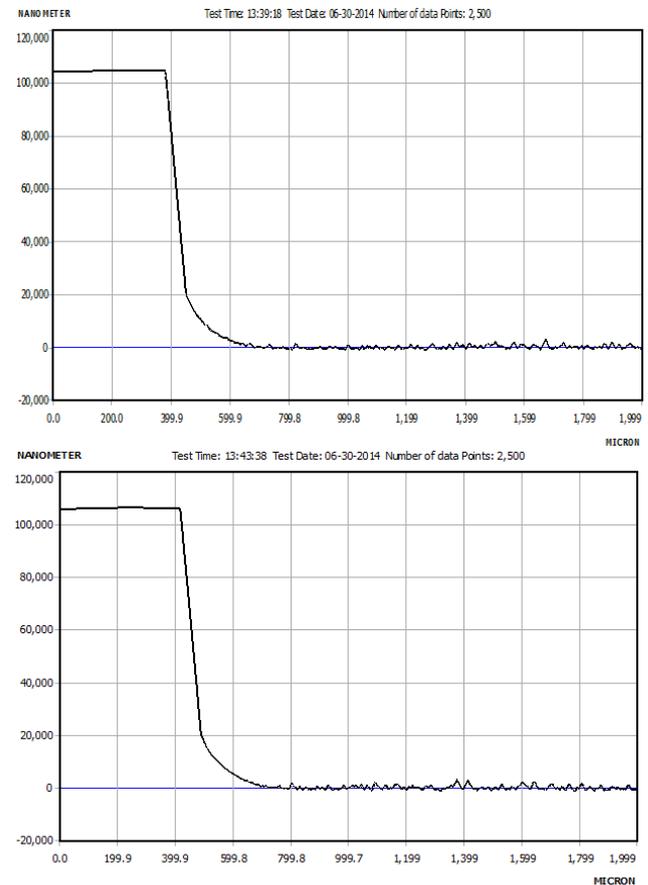


Figure 14. Surface profiles of two sides of etched 40μm deposited wafer after 1 hour of RIE

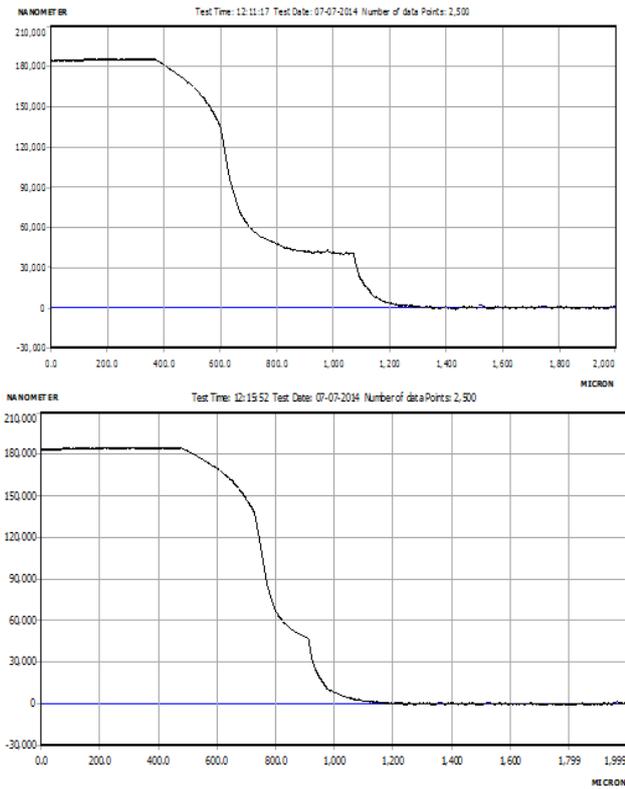
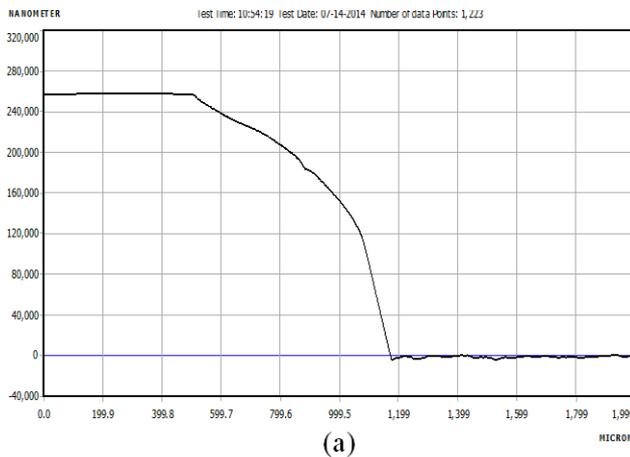
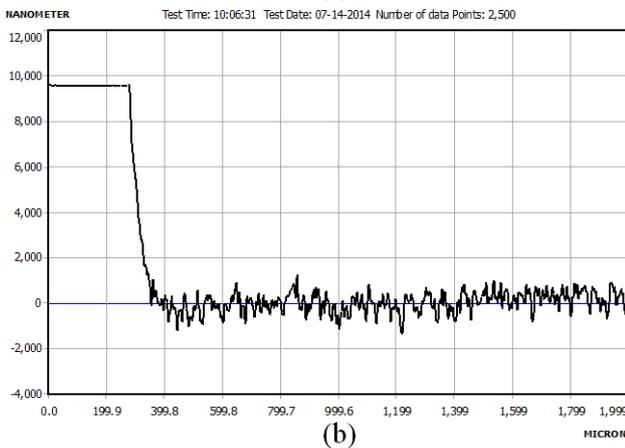


Figure 15. Surface profiles of two sides of etched 40 μm deposited wafer after 2 hours of RIE



(a)



(b)

Figure 16. (a) Surface profiles of total wafer thickness (b) Surface profile of extra 10 μm etch into supporting substrate

After another one hour, the etch depth was 184.9 microns after taking an average of measurements on two

sides of the etched window cavity as shown in Figure 15. After the third hour of etch, the wafer was completely etched and a depth of 10 microns into a supporting substrate used for placing the initial substrate in the RIE chamber to check the consistency of the etch rate. The surface profile was measured on two sides to determine the entire thickness of the wafer, the etch profile is shown in Figure 16 (a), and then measuring the etch depth of the supporting wafer as shown in Figure 16 (b).

The value of the etch depth of the second wafer was added to the entire thickness of the initial wafer and subtracting the previous etch after two hours, to determine the etch rates of the third hour. This value is depicted in equation 1.

$$X = (A + \delta) - B \quad (1)$$

Where A is the total thickness of the initial wafer, B is the etch depth after 2 hours and δ is the extra etch into the second wafer and X is the etch depth for the third hour. The value of the third etch after calculation using equation 1 was 85.7 microns [(260.6 + 10) – 184.9]. This means a total etch of 270.6 microns after three hours of RIE. The etch rates were calculated as 1.76 μm/min, 1.32 μm/min and 1.43 μm/min for the first hour, second hour and third hour respectively. These values were plotted as etch depth as a function of the etch time shown in Figure 17.

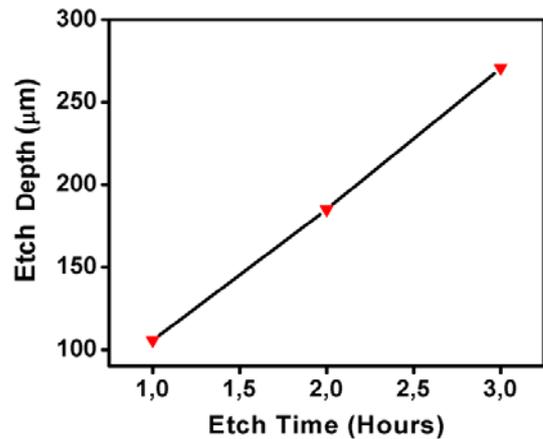
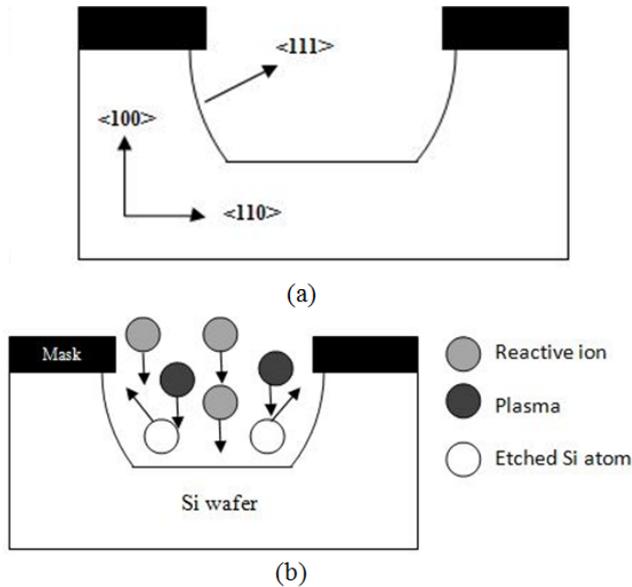


Figure 17. Etch rates of RIE on c-Si wafer after 1 hour, 2 hours and 3 hours

The etch rates fall within the range of 1.3 to 1.8 μm/min, with an average etch time of 1.5 μm/min. This means approximately 90 microns of etch for each hour, implying 3 to 5 times the etch rates of TMAH wet etching. The reason for faster etch rates is because of the synergy between the physical and chemical mechanisms occurring during RIE [12]. This effect is shown in Figure 18. The high energy collisions from ionization helps to dissociate etchant gases into more reactive nature resulting in a faster etch process [20]. RIE has other advantages like higher aspect ratio, this means more visible etch profiles [21]. There is little or no undercutting since the sidewalls are not exposed [22] when using this technique and after a deep etch, pinholes are not observed.

Some challenges with RIE were also noticed, relating more to the photoresist. As seen in the case of 120 μm deposition of SU-8, limited etch rates were observed on a full wafer because of problems with being held properly by the chamber clamp. In most cases, especially for 6 μm and 40 μm depositions, the photoresist was partially or

almost completely removed from the surface of the substrate. Another case was cracks observed on the SU-8 photoresist, making it more difficult to remove with 1-methyl-2-pyrrolidone. This increased the removal time from 1 – 2 hours to 3 – 5 hours. The etched surface is rougher than the TMAH etched surface. RIE has lower selectivity with the SU-8 photoresist of 50 – 75 to 1.



**Figure 18.** (a) Bow Anisotropic Etch profile of RIE showing crystallographic orientations (b) The Effect of the synergy between the physical and chemical mechanisms during RIE

## 4. Conclusions

The article develops reliable procedures to deeply etch silicon wafers to a thickness less than 20 $\mu\text{m}$  for fabricating IBC solar cells. A baseline photolithography process using SU-8 photoresist was developed. A study on the behavior of this type of photoresist and an influence of masked photolithography and etching was carried out. SU-8 photoresist is proven to be made harder by UV irradiation. It has higher aspect ratio imaging characteristics. Different thickness studies were carried out on this type of photoresist, 6 $\mu\text{m}$ , 40 $\mu\text{m}$  and 120 $\mu\text{m}$  depositions.

Etching techniques, TMAH wet anisotropic etching and RIE for silicon wafer thinning to ultra thin sizes have been investigated. The etch rates of RIE technique proved to be 3 to 5 times faster than the etch rates of TMAH with less disadvantages such as pinholes and cracks along the crystallographic planes. This indicates less breakage and better potential cell yield. The RIE proves capable of achieving smaller feature sized microstructures and good for future applications like the ultra thin interdigitated back contact solar cells. These reliable procedures speeds up fabrication process and reduces the cost of miniaturization.

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