

# Design of an Efficient Dedicated Low Power High Speed Full Adder

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**Abstract** In this paper, we have designed an efficient full adder with high speed & low power. As day by day more complex arithmetic circuits are presented, the power consumption becomes more important. Increasing demand for fast growing technologies in mobile electronic devices such as cellular phones, PDA's and laptop computers requires the use of a low-power Full Adder in VLSI system. One way to reduce the power by reducing the power. However, decreasing power supply increases the circuit's delay which is in contrast with high speed. So the power delay product (PDP) represents a trade-off between two compromising feature of power dissipation and circuit delay. The new high speed high performance full adder is implemented by using CMOS technology. Simulation has been carried out on "MENTOGRAPHICS TOOLS" on 250 nm technology. Modification was done to optimize W/L ratio with different power supply. Results were compared with previously done single bit full adder circuit in terms of power, delay and power delay product (PDP).The results involves better performance compared to traditional adders.

**Keywords:** PDA, CMOS, VLSI, PDP, NMOS

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## 1. Introduction

The performance of many applications such as digital signal processing depends on the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation and digital filtering. Usually, the performance of the integrated circuits is influenced by how the arithmetic operators are implemented in the cell library provided to the designer and used for synthesizing. As more complex arithmetic circuits are presented each day, the power consumption becomes more important. The arithmetic circuits grows more complex with the increasing processor bus width, so energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on a chip and faster clock. Increasing demand for fast growing technologies in mobile electronic devices such as cellular phones, PDA's and laptop computers requires the use of a low-power Full Adder in VLSI systems since it is the core element of arithmetic circuits. Decreasing the power supply leads to power consumption reduction [1]. However, lowering supply voltage also increases circuit delay and degrades drivability of cells designed with certain logic styles. One way of consuming less power is that a circuit operates at extremely low frequency, but it may take a very long time to complete which is in contrast with high speed operation demands. A specific task of our work is to make a comparison of the power consumption

of the Full Adders designed with different logic styles. We measured the energy consumption by the product of average power and worst case delay. The power-delay product (PDP) represents a trade-off between two compromising features of power dissipation and circuit latency [2].

## 2. Cmos Implementation of Full Adder

The full adder cell has been realized using 28T (conventional full adder) and has been shown in figure 2.2 The CMOS structure combines PMOS pull up and NMOS pull down network to produce considered output. It has the advantage of full output voltage swing. The drawback of this circuit is that it accures large silicon area and consumes more power. Therefore it is not suitable for low power area efficient applications [3].

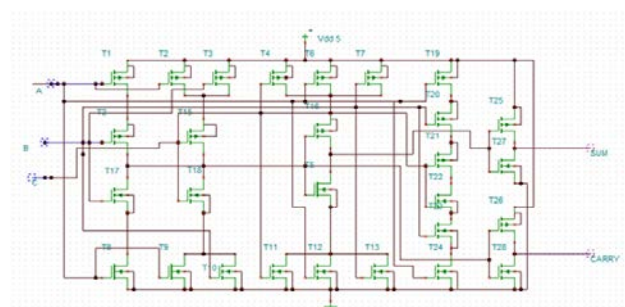


Figure 2.1. circuit diagram of CMOS implementation of 1 bit Full adder

## 2.1 Min FA

Min FA is a minority based full adder. Which uses 34 no of transistors. Although this is a low power CMOS based design, it has long critical path and not a high driving capability at the sum output, which leads long propagation delay.

### CIRCUIT DIAGRAM

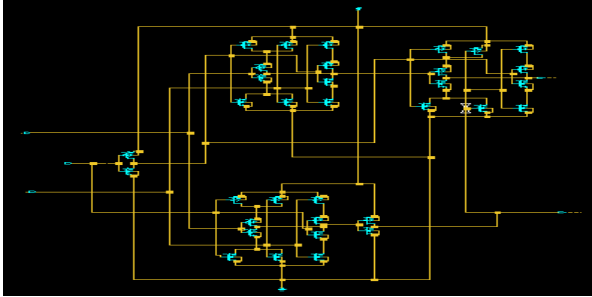


Figure 2.2. Circuit diagram of minority based full adder

## 2.2 Complementary & Level Restoring Carry Logic

The logic function of full adder can be represented as

$$\text{Sum} = (A \odot B) \cdot \text{Cin} + (A \oplus B) \cdot \text{Cin} \quad (2.1)$$

$$\text{Cout} = (A \oplus B) \cdot \text{Cin} + (A \odot B) \cdot A \quad (2.2)$$

From equation 2.1 and equation 2.2 we can easily identify that two basic modules needed to implement the function I.e. XOR and 2-1-Multiplexer. An XOR/XNOR function can easily implemented by using 4 transistor in pass transistor logic. A 2-1 multiplexer can also be implemented by using as few as 2 transistors if complimentary control signals are available. This complimentary and level restoring carry logic [9] is used to reduce circuit complexity and to archive faster cascade operation. This circuit is based upon the logic operation as follows

$$\text{Sum} = (A \oplus \text{Cin}) \cdot \text{Cout} + (A \odot \text{Cin}) \cdot B \quad (2.3)$$

$$\text{Cout} = (A \oplus \text{Cin}) \cdot B + (A \odot \text{Cin}) \cdot A \quad (2.4)$$

## 2.3. Circuit Description

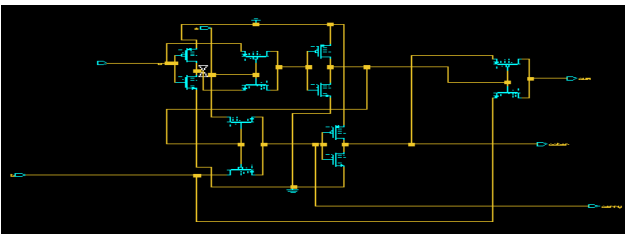


Figure 2.3. Circuit diagram of complementary and level restoring carry logic

According to Elmore formula, the propagation delay is a quadratic function of cascaded pass transistor. Even for moderate no of cascade length delay is intolerable. The XNOR circuit used in this circuit is realised by using 2 to one multiplexer followed by an inverter. The inverter plays vital role in this circuit Firstly it is used as a level restoring circuit to combat the output threshold voltage

loss. the level restored output is then feed to MUX 2/3 to generate sum and Cout signal, Secondly the (inverter 2) serves as buffer along the carry chain to speed up the carry propagation. Thirdly the inverter 2 provides complimentary signal (c out) needed in the following stage [4]. The complimentary signal also helps in to simplify the XNOR operation where only one signal is needed in the selection control. The MOS schematic circuit is presented below which uses only 12 transistor.

## 3. Minority Function Bridge Style Full Adder Circuit Description

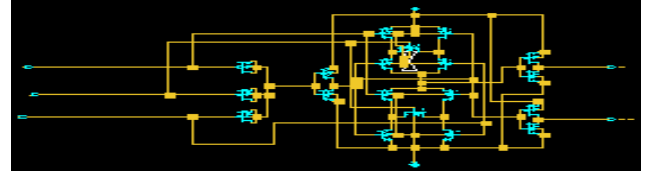


Figure 3.1. Circuit diagram of minority function bridge style full adder

The new adder module consists of three capacitors to perform voltage summation to implement scaled linear sum. This module takes minority function as well as bridge style to implement sum and carry. Although the new design uses capacitive network, this design is totally different from previous one [5] Bridge circuit provides conditional conjunction between two circuit nodes. Since one of the important parameter in the circuit design is the chip area. The bridge style reduces chip area or increase density of transistor in the unit of area [6]. Circuits can be implemented faster and smaller than conventional adder circuit, Bridge circuit makes it possible to create a new path from supply lines to an output through sharing transistor of different paths. These transistors are arranged in such a way that validates the connection of the circuits and also preserves pull up and pull down network mutually exclusively [7].

Table 1. Implementation of  $\overline{\text{Sum}}$  and  $\overline{\text{Cout}}$

A	B	C	$\overline{\text{Cout}}$	Min(A,B,C)	$\overline{\text{Sum}}$
0	0	0	1	1	1
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	0

The minority function acts as follows: If the no of "0"s becomes greater than no of "1"s at the i/p's, the output will be "1". Minority is a function of odd number of inputs [8]. This module is designed using a 3-i/p Minority circuit, followed by bridge style. The functionality of the new design is based on the following equation

$$\overline{\text{Sum}} = \overline{\text{Cout}} (A + B + C) + ABC_{in} \quad (3.1)$$

$$\overline{\text{Cout}} = \text{Minority}(A, B, C_{in}) \quad (3.2)$$

This means that  $\overline{\text{Cout}}$  function can be implemented by minority circuit, and the  $\overline{\text{Sum}}$  function can be implemented using  $\overline{\text{Cout}}$ .

### 4. Experimental Result and Analysis

The proposed design is simulated by using mentographic tools with 250 nm technology at room temp. i.e 27°C. In this experiment we have adjusted the aspect ratios I.e (W/L) of both PMOS and NMOS transistors so as to get the accurate results.

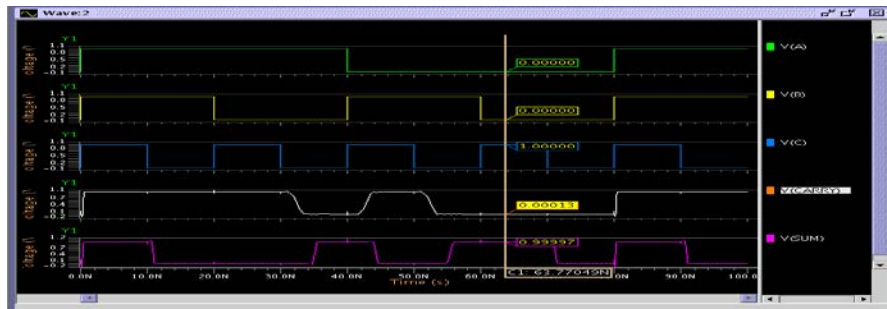
The design is also simulated at different power supply voltage ranging from 0.7v to 1v and corresponding delay is measured with the target to reach less power delay product (PDP) I.e. energy.

#### 4.1. Power Comparison

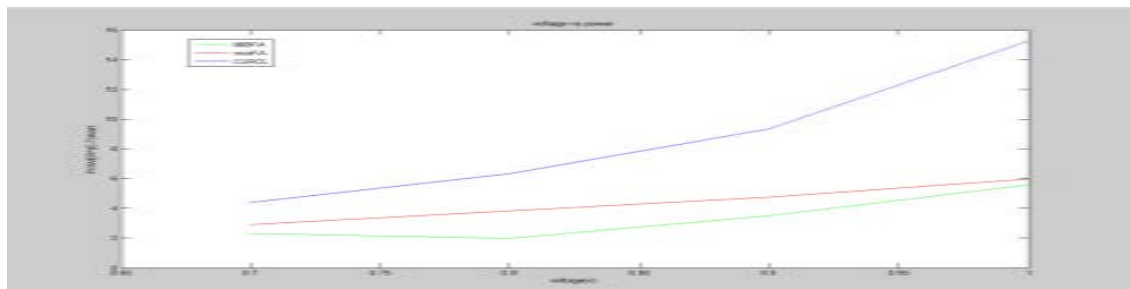
The average power consumption is also measured by applying a complete pattern during a long period of time. In this experiment, the adder cells are simulated at 250 nm feature size by varying supply voltages ranging from 0.7v to 1v with 0.1v as step size.

**Table 2. Comparison between power supply and power consumed**

Name of adder cell	0.7v	0.8v	0.9v	1v
Min fa	2.5713	3.442	4.2532	5.8219
CLRCL	4.4068	6.3375	9.3354	15.2779
MBFA	2.3198	2.8333	3.500	5.8743



**Figure 4.1.** Experimental result of minority based full adder with bridge style



**Figure 4.2.** Graph between power supply and power consumed

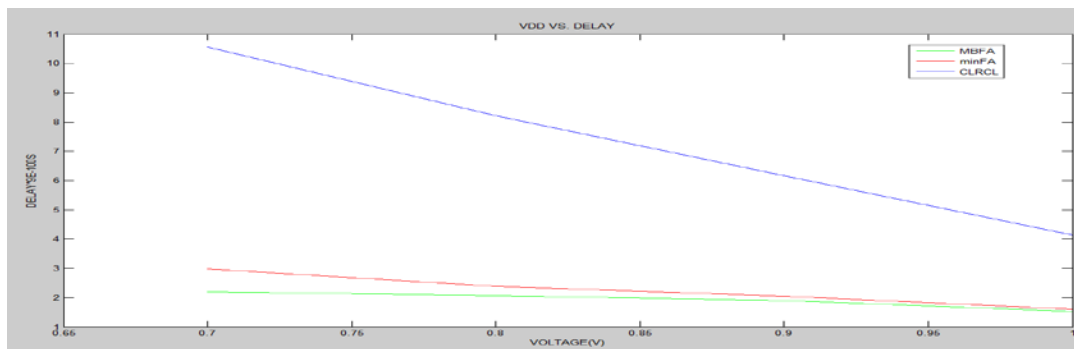
#### 4.2. Delay Comparison

For each transition, delay is measured from 50% of the input voltage swing to the 50 % of the output voltage swing. The maximum delay is taken as the cell delay. Our design has short critical path[9] for generating sum and Cout and has smallest delay among all the designs. The delay is also measured by applying a complete pattern during along period of time. In this experiment, the adder

cells are simulated at 250nm feature size by varying supply voltages ranging from 0.7v to 1v with 0.1v as step size.

**Table 3. Comparison between power supply and delay**

Name of adder cell	0.7v	0.8v	0.9v	1v
minFA	2.9836	2.3876	2.0608	1.5994
CLRCL	10.5650	8.2220	6.1760	4.130
MBFA	2.2024	2.0654	1.8956	1.5234



**Figure 4.3.** Graph between power supply and delay

#### 4.3. Power Delay Product Comparison

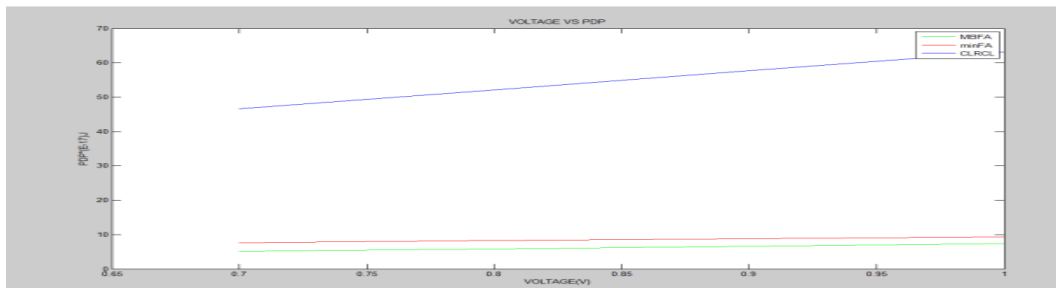
The PDP is a qualitative measure of efficiency and compromise between power dissipation and speed. PDP

is particularly important When low power operation is needed. The average power consumption and average delay is calculated to find the energy required for the proper operation of the circuit is calculated and tabulated

as below. As per the results, the delay of the proposed design increases approximately in a linear manner by increasing the number of modules. In addition to it, the power of proposed design increases slowly with the increase of the number of modules.

**Table 4. Comparison between power supply and PDP Simulation result at 250 nm technology**

Name of adder cell	0.7v	0.8v	0.9v	1v
minFA	7.6719	8.2185	8.7651	9.3117
CLRCL	46.5580	52.1070	57.656	63.2050
MBFA	5.1092	5.8520	6.6348	7.3977



**Figure 4.4.** Graph between power supply and PDP

From the above graph it is seen that MBFA has lowest PDP among three adder designs. The design having lowest PDP is very energy efficient.

considering the PDP(energy) the new design is more efficient than other designs.

#### 4.4. No. of Transistor Comparison

By taking the area concept the no of transistors used are compared in different logic style. Although the no of transistors used in minority based full adder with bridge style is somehow higher than CLRCL [9] it gives lower PDP. which is most required for high speed as well as low power consumption. It is obvious that it uses less no of transistors than minority based full adder. So it uses less silicon area than minority based full adder.

**Table 5. Comparison between No. of transistors used**

Adder cells	No. of transistors used
minFA	34
CLRCL	12
MBFA	17

#### 5. Conclusion

In this paper the comparison of the three distinct adder architectures, the minority based full adder with bridge style adder is shown to be vastly superior in terms of circuit speed over virtually all testing conditions. Power analysis subsequently showed that the new design dissipated the more power than minority based full adder but it consumes less power than CLRCL adder. Although the silicon area consumed by CLRCL is less, by

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