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High Gain, Two-Stage, Fully Differential Audio Amplifier with 0.18μm CMOS Technology

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Abstract The two-stage, fully differential audio amplifier with 0.18μm CMOS technology and TSMC process is proposed. Telescopic amplifier created stage one and common emitter structure used to provide high gain in stage two. The amplifier has a ±1.2V differential output swing and a gain greater than 127dB while consuming power less than 10mW from 1.8V supply voltage. The step response of the audio amplifier is about 0.04us and the gain-bandwidth of the circuit is near 1.1GHz. Hspice software used to produce simulation results.

Keywords: *telescopic , fully differential amplifier , 0.18μ CMOS technology, two-stage audio amplifier*

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1. Introduction

With decreasing channel length, CMOS technology becomes an attractive candidate for integrated circuits [1]. Usually the operational amplifier is the block with the highest power consumption in analog integrated circuits in many applications. Low power consumption in circuits is becoming more important in handset devices, so it is a challenge to design a low power amplifier. There is a trade off among speed, power and gain for an amplifier design because usually these parameters are called contradicting parameters [2]. Usually three kinds of operational amplifier exist: two-stage, folded-cascode and telescopic. The telescopic amplifier consumes the least power as compared with the other two amplifiers, so it is widely use in low-power consumption applications [3,4]. A lower current (which follows in differential pair transistors) can improve small-signal resistance of transistors and increase the amplifier's gain. Recently, telescopic amplifier design and research focused on improving gain and output swing [5,6]. One of the telescopic amplifier disadvantages is severely limited output swing. In this paper high-gain and low-power fully differential audio amplifier based on telescopic and common emitter structure is proposed. The circuit has a high output swing and gain-bandwidth. Hspice software and 0.18μm CMOS technology and TSMC process used to produce simulation results. This circuit is suitable for on-chip integrated audio amplifier in the communication system.

2. Design of Two-stage Amplifier

Figure 1 shows the complete circuit of the two-stage fully differential audio amplifier. The NMOS telescopic amplifier transistors (M1-M4) have the same characteristics such as w, l, AD, AS, PD, PS and … (This is also applied for PMOS (M5-M8) transistors). The emitters of M7 and M8 are connected to VDD. Eq. (1) describes the maximum allowable current consumes from a 1.8V supply voltage of the amplifier.

$$It\max = \frac{P\max}{VDD} \tag{1}$$

$$Itran = I1 + I6 + I7 \tag{2}$$

$$Ibais = I2 + I3 + I4 + I5 \tag{3}$$

$$It\max = Itran + Ibais \tag{4}$$

It depends on designer to assign these currents. Then the designer must obtain the telescopic amplifier transistor's dimensions. (In equations V_{OD}, Cox, V_T and μ are:

V_{OD}: overdrive voltage,
Cox: gate oxide capacitor,
V_T : threshold voltage,
μ: electron or hole mobility)

$$|V_{OD}| = |V_{GS}| - |V_T| \tag{5}$$

$$K' = \frac{1}{2}\mu COX \tag{6}$$

$$\sum |V_{OD}| = V_{DD} - \frac{swing}{2} \tag{7}$$

$$\begin{aligned} V_{OD1} + V_{OD3} + |V_{OD5}| + |V_{OD7}| &= V_{DD} - \frac{swing}{2} \\ V_{OD2} + V_{OD4} + |V_{OD6}| + |V_{OD8}| &= V_{DD} - \frac{swing}{2} \end{aligned} \tag{8}$$

Because of similarity:

$$V_{OD1} = V_{OD3} = V_{OD2} = V_{OD4} \tag{9}$$

$$|V_{OD5}| = |V_{OD6}| = |V_{OD7}| = |V_{OD8}| \tag{10}$$

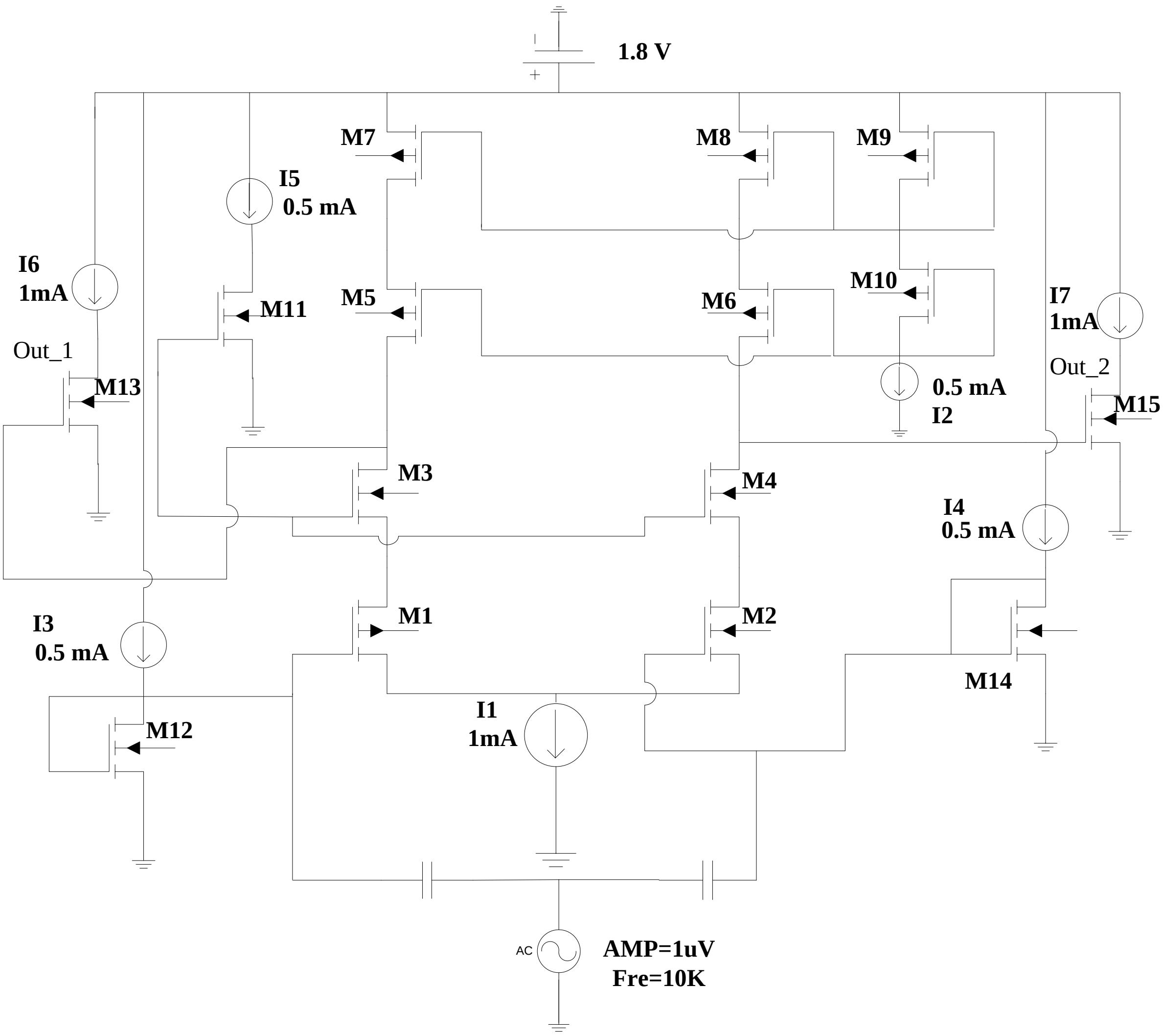

Figure 1. The two-stage, fully differential audio amplifier with biasing circuit

By assigning suitable voltages to V_{OD1} and $|V_{OD5}|$, telescopic amplifier transistor's dimensions can be calculated. Usually in Eq. (11) K'_n is not equal to K'_p ($K'_n \geq K'_p$). The designers should notice this issue, when they consider the values for overdrive (V_{OD}) voltages (W: MOSFET channel width, L: MOSFET channel length).

$$\left(\frac{W}{L}\right) \cong \frac{I_D}{K' \times (V_{OD})^2} \tag{11}$$

Because of using the same characteristics for M1-M4 and M5-M8:

$$W_1 = W_2 = W_3 = W_4 \tag{12}$$

$$W_5 = W_6 = W_7 = W_8 \tag{13}$$

$$L_1 = L_2 = L_3 = L_4 \tag{14}$$

$$L_5 = L_6 = L_7 = L_8 \tag{15}$$

For calculating MOSFET's dimensions such as:
1-AD: Drain diffusion area
2-AS: Source diffusion area
3-PD: Perimeter of the drain junction
4-PS: perimeter of the source junction

Eq. (16) and (17) used.

$$AD = AS \cong W \times L_S \tag{16}$$

$$PD = PS \cong 2W + 2L_S \tag{17}$$

L_S (in Eq. (16) and (17)) depends on technology, for example for 0.18µm COMS technology L_S is 0.48µm or for 0.13µm CMOS technology it is 0.55µm. M9-M11 used to bias circuit. Note that all of the transistors should be biased in the saturation region. To achieve this issue the designer should consider saturation's conditions. Solving Eq. (11) requires K' initial value. For finding this value, two methods suggested:

First- Simulate a simple circuit includes a transistor with the same amplifier transistor's characteristics and using simulation results for finding K'.

Second- Utilize company's test results about CMOS technology (e.g. MOSIS). Table 1 displays MOSIS simulation results for K'.

Table 1. MOSIS Parametric Test Results

RUN	K'n(uA/V^2)	K'p(uA/V^2)
T42P(MM_NON-EPI)	173.1	-35.9
T58F (MM_NONEPI_THK-MTL)	172.8	-36

After finding MOSFET's aspects ratio (W/L), transistor's transconductance (g_m) can be calculated from Eq. (18).

$$gm = \sqrt{\mu.Cox.\frac{W}{L}.2.I_D} \tag{18}$$

Consequently, One-sided gain is obtained from Eq. (22) (r_o is drain-source resistance in MOSFET's small-signal equivalent circuit).

$$A_{V\ telescopic} = -gm_1(r_{on} \,||\, r_{op}) \tag{19}$$

$$r_{on} = r_{o3}(1+gm_3.r_{o1}) \tag{20}$$

$$A_{V\ common\_emitter} = -gm_{16}\ (r_{o16}) \tag{21}$$

$$A_{V\ total} = A_{V\ telelescopic} \,.\, A_{V\ common\_emitter} \tag{22}$$

3. Circuit Specification's Goals

The circuit's specifications goals (that we should be achieved) are:

1- 1.8V supply voltage.
2- Power consumption less than 10mW.
3- Gain higher than 90dB.
4- Differential output swing higher than 2.4V (1.2V one-sided output swing).
5- Sinusoidal input voltage with 1μv peak to peak amplitude.

4. Simulation Results

Table 2 displays the fully differential audio amplifier transistor's dimensions. Eq. (23) and (24) described The currents consumption of the amplifier circuit.

$$I1 = I6 = I7 = 1mA \tag{23}$$

$$I2 = I3 = I4 = I5 = 0.5mA \tag{24}$$

Table 2. Transistor's Dimensions

	L(um)	W(um)	AD,AS(pm)	PD,PS(um)
M1-M4	0.18	291.8	140.6	584.5
M5-M8	0.18	309.5	148.56	619.96
M13,M15	0.67	291.8	140.06	584.56
M9,M10	0.5	309.5	148.56	619.96
M12,M14	1	129.6	62.2	260.16
M11	0.5	7	3.36	14.96

Table 3 shows MOSFET's parameters simulation results.

Process and model Specifications:
TSMC RF SPICE MODEL
This model has been modified for RF purpose.
Process: 0.18μm Mixed-Signal
SALIIDE (1P6M+, 1.8V/3.3V)
Model: BSIM3 (V3.24)
DOC. NO: T-018-MM-SP-001
VERSION: 1.3.1

Table 3. MOSFET's parameter's Simulation Results

	Id (uA)	Vgs (mV)	Vds (mV)	Vth (mV)	Vdsat (mV)	gm 1/(mΩ)	gds 1/(uΩ)	region
M1,M2	500	510.70	280.92	449.67	115.53	7.57	49.00	saturation
M3,M4	500	586.68	183.11	523.68	117.43	7.46	186.07	saturation
M5,M6	-500	-727.27	-727.29	-598.82	-153.19	5.77	16.49	saturation
M7,M8	-500	-562.28	-562.28	-438.35	-145.48	5.87	22.41	saturation
M9	-500	-562.28	-562.28	-438.35	-145.48	5.87	22.41	saturation
M10	-500	-727.27	-727.27	-598.82	-153.19	5.77	16.49	saturation
M12,M14	500	557.08	557.08	436.43	157.95	5.83	14.86	saturation
M13,M15	997.66	510.41	208.86	436.08	123.01	14.07	107.16	saturation
M11	500	913.99	913.99	436.37	400.28	1.67	14.48	saturation

Figure 2 represents one-sided output signals simulation result (out_1 and out_2) which is compatible with Eq. (22). Step response is the time behavior of the outputs of a general system when its inputs change from zero to one in a very short time. The concept can be extended to the abstract mathematical notion of a dynamical system using an evolution parameter. From a practical standpoint, knowing how the system responds to a sudden input is important because large and possibly fast deviations from the long term steady state may have extreme effects on the component itself and on other portions of the overall system dependent on this component. In addition, the overall system cannot act until the component's output settles down to some vicinity of its final state, delaying the overall system response. Formally, knowing the step response of a dynamical system gives information on the stability of such a system, and on its ability to reach one stationary state when starting from another. The step response of the fully differential audio amplifier is displayed in Figure 3. Figure 4 describes the structure used for simulating the step response of the audio amplifier. Frequency response is the quantitative measure of the output spectrum of a system or device in response to a stimulus, and is used to characterize the dynamics of the system. It is a measure of magnitude and phase of the output as a function of frequency, in comparison to the input. In simplest terms, if a sine wave is injected into a system at a given frequency, a linear system will respond at that same frequency with a certain magnitude and a certain phase angle relative to the input. Two applications of frequency response analysis are related but have different objectives. For an audio system, the objective may be to reproduce the input signal with no distortion. That would require a uniform (flat) magnitude of response up to the bandwidth limitation of the system, with the signal delayed by precisely the same amount of time at all frequencies. That amount of time could be seconds, or weeks or months in the case of recorded media. The frequency response and gain-bandwidth value of the fully differential audio amplifier are shown in Figure 5. AC simulation results include:

One-sided output swing: [1.24 V]

Two-sided output swing: [(2×1.24=2.48)]

Power consumption: [(I1+I2+I3+I4+I5+I6+I7)×VDD=(1m+ 0.5m+0.5m+0.5m+0.5m+1m+1m)×1.8=9mW]

Tow-sided output gain:

$$Av \cong \frac{2.4V}{1\ \mu V} = 2400000 = 127.6\ dB \qquad (25)$$

MOSFET’s parameters simulation results are presented in Table 3. Table 4 describes simulation results briefly.

Table 4. Output Swing, Gain and Power Results

	Goal	Result
Two-sided swing	2.4V	2.4 V
Two-sided gain	≥90 dB	127.6 dB
Power consumption	≤10mW	9 mW
Gain-bandwidth		1 GHz
Settling time		0.04 us

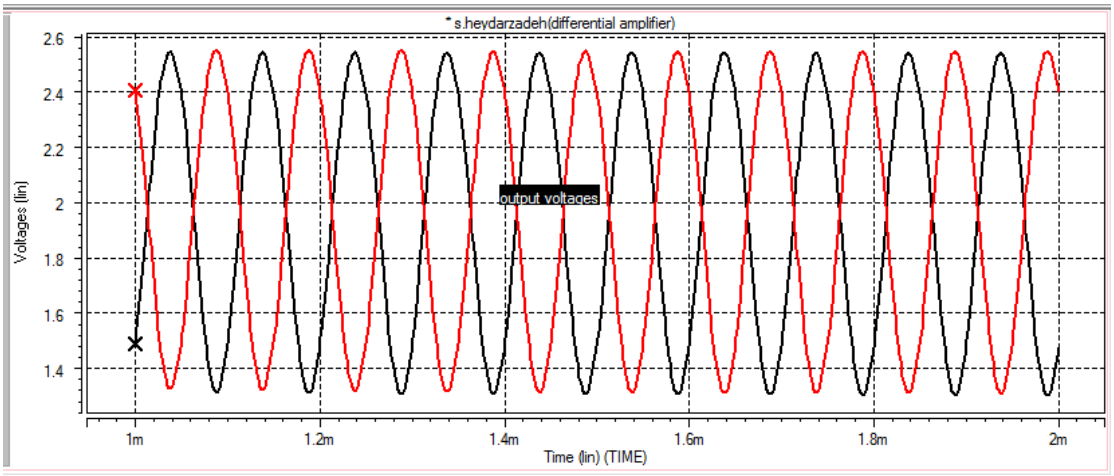

Figure 2. One-sided output signals (out_1,out_2)

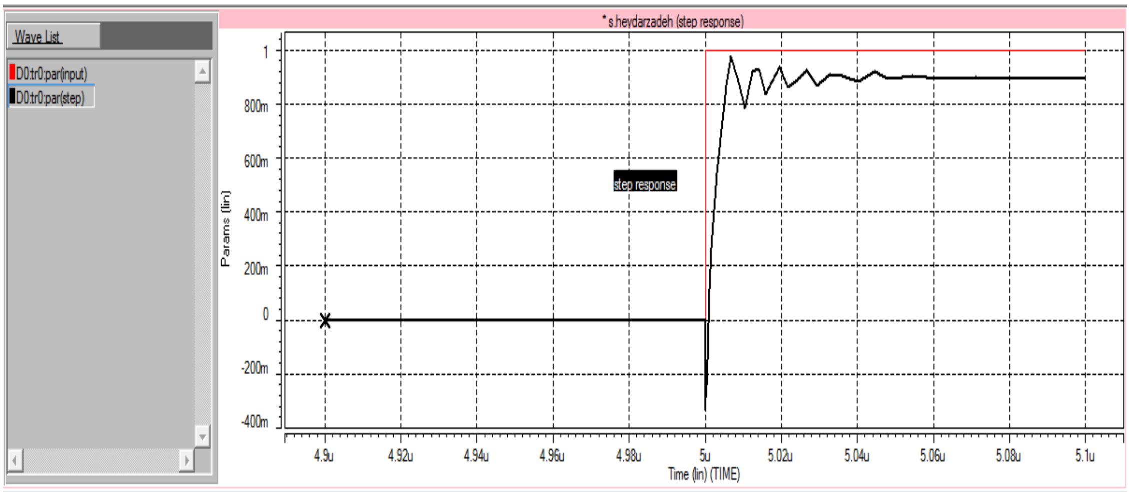

Figure 3. Fully differential audio Amplifier step response

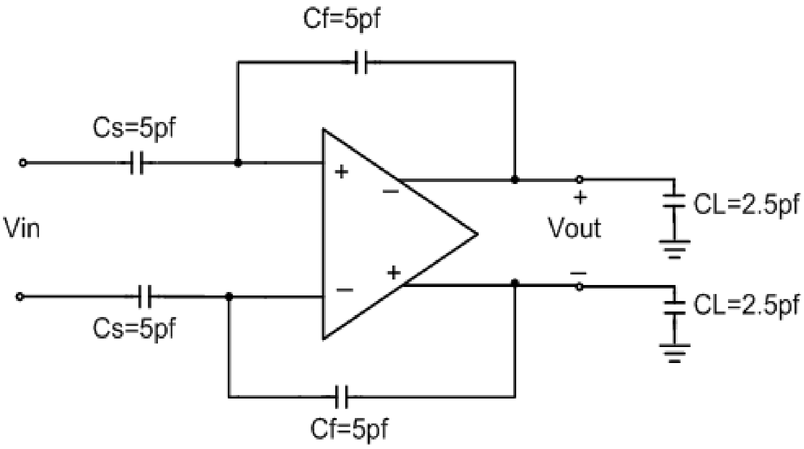

Figure 4. Amplifier step response structure

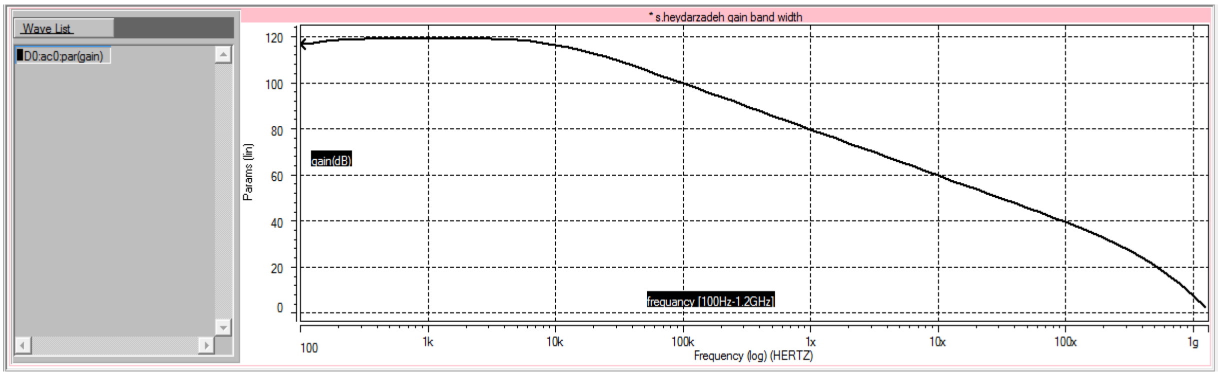

Figure 5. Amplifier Frequency response (AC simulation form 100Hz-1.2GHz)

5. Conclusion

A two-stage fully differential audio amplifier has been successfully designed and simulated. With this method and process, we achieved a gain greater than 127dB and the output swing about 2.4V from 1uV sinusoidal input voltage. The circuit consumes power less than 10mW from 1.8V supply voltage. The step response of the audio amplifier is about 0.04us that is suitable for on-chip amplifier in microphone. The gain-bandwidth of the audio amplifier is near a 1.1GHz and the frequency response curve shows that audio signals with 20kHz bandwidth can be amplified with high gain. The proposed structure is a suitable for low-power, small area occupation and high gain on-chip integrated audio amplifier in communication system.

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